

REMARKS

This is intended as a full and complete response to the Office Action dated May 5, 2004, having a shortened statutory period for response extended one-month to expire on September 7, 2004. Claims 1-17 and 40-55 remain pending in the application and are shown above. Claims 1-17 and 40-55 stand rejected by the Examiner. Applicants cancel claims 44 and 54 without prejudice. Reconsideration of the rejected claims is requested for reasons presented below.

Claims 1-11 stand rejected under 35 U.S.C. § 112, second paragraph, as failing to comply with the written description requirement. Claim 1 has been amended to clarify the invention. These amendments are not presented to distinguish a reference, thus, the claims as amended are entitled to a full range of equivalents if not previously amended to distinguish a reference. Withdrawal of the rejection is respectfully requested.

Claims 1-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Liu, et al.* U.S. Patent No. 6,225,223. The Examiner asserts that *Liu, et al.* discloses depositing a first copper layer on a barrier layer to fill a feature definition, planarizing the first copper layer and barrier layer to re-expose the dielectric layer, selectively depositing a second copper layer on the now dished first copper layer, and planarizing the second copper layer. The Examiner further asserts that the difference between the prior art and the instant claims is elective etching and it would have been obvious to one of ordinary skill in the art to determine through routine experimentation the optimum, operable etch type in *Liu, et al.* the aspects of the invention recited in claims 1-7. Applicants respectfully respond to this rejection.

Liu, et al. discloses a method of forming an interconnect including forming a barrier layer over a dielectric layer, depositing a first copper layer on the barrier layer to fill a trench, polishing both the first copper layer and barrier layer to expose the upper surface of the dielectric layer and forming a dished copper filled trench, and selectively depositing a second copper layer over the dished copper filled trench. (See, col. 2, lines 5-23, col. 3, line 30 to col. 4, line 18, and Figures 1-4).

Thus, the method of *Liu, et al.* requires polishing both the first copper layer and barrier layer to expose the surface of the dielectric layer and dished copper filled trench in order to selectively deposit a second copper layer over the dished copper filled trench. Applicants respectfully point out that *Liu, et al.* discloses polishing only the second copper layer in order to form a planar copper filled trench.

Applicants respectfully disagree with the Examiner's assertion that polishing the first conductive material to the barrier layer, then depositing the second conductive material to fill recesses formed in the first conductive material, and then polishing the barrier layer is an optimization of the combined copper and barrier etching process of *Liu, et al.* There is no suggestion or motivation in *Liu, et al.* to optimize a process outside of the scope of *Liu, et al.*

Therefore, *Liu, et al.* does not teach, show, or suggest polishing the first conductive material to a top surface of the barrier layer material, depositing a second conductive material by an electrochemical deposition technique on at least the first conductive material to fill recesses formed in the first conductive material, and polishing the second conductive material and the barrier layer material to at least a top surface of the dielectric layer to form a planar surface, as recited in claim 1 and claims dependent therefrom. Withdrawal of the rejection is respectfully requested.

Claims 8-10 stand rejected under 35 U.S.C. § 103(a) as being obvious over *Liu, et al.* as applied to claim 1 above, and further in view of *Lacoponi, et al.* (U.S. Pat No. 6,489,240). The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the annealing and rinsing steps taught by *Lacoponi, et al.* in the process taught by *Liu, et al.* Applicants respectfully respond to this rejection.

Liu, et al. has been discussed above. *Lacoponi, et al et al.* discloses a method of forming a copper interconnect having multiple dielectric layers and multiple copper layers. The method of *Lacoponi, et al.* includes forming a copper seed layer 525B and a copper layer 640, and annealing the copper layer 640 using a rapid thermal anneal process or a furnace anneal process (See, col. 5-6). In addition, *Lacoponi, et al.* discloses the use of intermediate tools for performing various steps involved after the overall copper interconnect is formed, such as cleaning, rinsing, and forming additional

layers (See, col. 9, line 66-67). Further, *Lacoponi, et al.* also discloses etching a roughened surface of a copper portion 740 by a selective etchant and depositing a thin copper layer 1100 above the copper portion 740. (See, col. 8, lines 60-67)

The combination of *Liu, et al.* and *Lacoponi, et al.* does not teach, show, or suggest providing a substrate with feature definitions formed in a dielectric material, depositing a barrier layer material on a substrate surface and in the feature definitions, depositing a first conductive material on the barrier layer material to fill the feature definitions, polishing the first conductive material to a top surface of the barrier layer material, depositing a second conductive material by an electrochemical deposition technique on at least the first conductive material to fill recesses formed in the first conductive material, and polishing the second conductive material and the barrier layer material to at least a top surface of the dielectric layer to form a planar surface, as recited in claims 1 and claims dependent therefrom including claims 8-10. Applicants respectfully request withdrawal of the rejection.

Claims 11-17 and 40-55 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Liu, et al.* U.S. Patent No. 6,225,223 in view of *Lacoponi, et al.* and further in view of *Zhang*, (U.S. Pat. No. 6,341,998). The Examiner asserts that it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the concurrent deposition and polishing method as taught by *Zhang* in the process taught by the combination of *Lacoponi, et al.* and *Liu, et al.* Applicants respectfully respond to this rejection.

Liu, et al. and *Lacoponi, et al.* have been discussed above. *Zhang* discloses an apparatus and a method for concurrent copper plating and polishing the plated copper on some portions of a wafer using a polishing pad to impede copper plating and facilitate plating/deposition in other desired locations of the wafer surface, such as an interconnect trench. There is no suggestion or motivation in the concurrent plating and polishing process of *Zhang* or *Liu, et al.* to modify the copper and barrier polishing process of *Liu, et al.* and the post-polish copper deposition of *Liu, et al.* to be performed in a concurrent depositing and polishing process.

The combination of *Liu, et al.*, *Lacoponi, et al.*, and *Zhang* do not teach, show, or suggest providing a substrate with feature definitions formed in a dielectric material,

depositing a barrier layer material on a substrate surface and in the feature definitions, depositing a first conductive material on the barrier layer material to fill the feature definitions, polishing the first conductive material to a top surface of the barrier layer material, depositing a second conductive material by an electrochemical deposition technique on at least the first conductive material to fill recesses formed in the first conductive material, and polishing the second conductive material and the barrier layer material to at least a top surface of the dielectric layer to form a planar surface, as recited in claim 1, and claims dependent thereon including claims 40-46. Applicants respectfully request withdrawal of the rejection.

The combination of *Liu, et al.*, *Lacoponi, et al.*, and *Zhang* do not teach, show, or suggest providing a substrate with feature definitions formed in a dielectric material, depositing a barrier layer material on a substrate surface and in the feature definitions, depositing a first conductive material on the barrier layer material to fill the feature definitions, polishing the first conductive material to a top surface of the barrier layer material, depositing a second conductive material by an electrochemical deposition technique on at least the first conductive material to fill recesses formed in the first conductive material, and polishing the second conductive material and the barrier layer material to at least a top surface of the dielectric layer to form a planar surface, wherein depositing the second conductive material and polishing the second conductive material and the barrier layer material are performed concurrently, as recited in claim 11. Applicants respectfully request withdrawal of the rejection.

With regard to claim 12 and claims dependent therefrom, *Liu, et al.* discloses polishing only the second copper layer to form a planar copper filled trench and *Lacoponi, et al.* discloses etching only the copper portion 740 and depositing a thin copper layer 1100 to form a planar copper filled trench. *Zhang* discloses concurrent copper plating and polishing the plated copper. In addition, applicants respectfully point out that *Liu, et al.* discloses polishing the first copper layer and the barrier layer and exposing the dielectric layer before depositing the second copper layer and *Lacoponi, et al.* discloses annealing a copper layer, polishing the copper layer and a barrier layer, and exposing the dielectric layer before etching the copper layer. However, both references fail to teach, show, or suggest exposing the barrier layer to selectively

deposit a conductive material on the copper material over at least a top surface of the barrier layer. *Zhang* does not teach, show, or suggest polishing a copper material from the substrate surface to at least a top surface of the barrier layer material, which is lacking in *Liu, et al.* and *Lacoponi, et al.* and as recited in claim 12 and claims dependent therefrom.

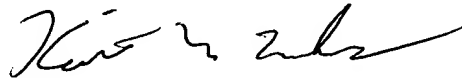
Thus, the combination of *Liu, et al.*, *Lacoponi, et al.*, and *Zhang* do not teach, show, or suggest providing a substrate to a polishing station disposed on a processing system, wherein the substrate comprises a dielectric material with substrate feature definitions formed therein, a barrier layer material disposed thereon and within the feature definitions, and a copper material disposed on the barrier layer material, polishing a copper material from the substrate surface to a top surface of the barrier layer material, transferring the substrate to an electrochemical deposition and polishing station disposed on the polishing system, depositing a conductive material on the copper containing material by an electroless deposition technique while removing the conductive material and the barrier layer material to at least a top surface of the dielectric layer by a polishing technique, as recited in claim 12 and claims dependent therefrom. Applicants respectfully request withdrawal of the rejection.

The combination of *Liu, et al.*, *Lacoponi, et al.*, and *Zhang* do not teach, show, or suggest providing a substrate to a polishing station disposed on a processing system, wherein the substrate comprises a dielectric material with substrate feature definitions formed therein, a barrier layer material disposed thereon and within the feature definitions, and a copper material disposed on the barrier layer material, polishing a copper material from the substrate surface to a top surface of the barrier layer material, depositing a conductive material on the copper material by an electrochemical deposition technique, polishing the conductive material and the barrier layer material to at least a top surface of the dielectric layer by a polishing technique, as recited in claim 47, and claims dependent thereon. Applicants respectfully request withdrawal of the rejection.

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the office action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

In conclusion, the references cited by the Examiner, alone or in combination, do not teach, show, or suggest the invention as claimed. Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



Keith M. Tackett
Registration No. 32,008
MOSER, PATTERSON & SHERIDAN, L.L.P.
3040 Post Oak Blvd. Suite 1500
Houston, TX 77056
Telephone: (713) 623-4844
Facsimile: (713) 623-4846
Agent for Applicant(s)

284094_1